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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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Optical receiver circuit

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Optical receiver circuit

The invention relates to an optical receiver circuit, in particular to an optical receiver circuit for CATV applications.

In the state of the art there are several attenuators well known for attenuation of an electrical signal. The US-A-5,448,207 discloses an attenuator circuit which has a small insertion loss and also as a broad tolerance with regard to the fluctuation of the element parameter. An attenuator stage having the largest attenuation quantity of a plurality of attenuator stages is formed with a Π-type attenuator stage, and an attenuator stage having the smallest attenuation quantity of the plurality of attenuator stages is formed with a T-type attenuator stage. In this way, an attenuator stage having a large attenuation quantity whose precision of the attenuation quantity is apt to be detracted is formed with a Π-type attenuator stage so that the precision becomes high, further, an attenuator stage having a small attenuation quantity is formed with a T-type attenuator stage so that the insertion loss can be lowered. This circuit is a so-called characteristic impedance network. This means that the input and output impedance of this attenuation circuit is constant, independent of an attenuation setting, and equal to the source and load impedance to have a good matching function.

The US-A-5,563,557 discloses an attenuator device comprising a unit step attenuator having a switch, an attenuation resistor connected in parallel to the switch and two shutdown resistors. Three current source circuits are provided having three transfer gates and three current source FETs for controlling a gate current of the switch FET. The signal transmission loss and the layout area can be reduced as much as possible, even if various attenuation rates are required. This circuit is also a characteristic impedance network. As described above, this means that the input and output impedance of this attenuation circuit is constant. The object of the US-A-5,563,557 is the signal transmission source, the frequency characteristic of the circuit and the attenuation rate of the circuit.

The JP-A-10-173464 discloses a step attenuator directed to minimizing a phase shift in a through state and an attenuation state. This attanuator is composed of

resistors, a MOSFET and a phase compensating circuit including resistors corresponding to an input terminal, an output terminal and control terminals, the resistors and the FET forms and attenuation switch setting circuit. The shift quantity of a passing phase at the time of passing operation and at the time of attenuation operation is restrained at a minimum via a control signal to the control terminal of the attenuation switch setting circuit and the control terminal of the phase compensating circuit.

The JP-A-07-249954 provides a step attenuator which is reduced in its insertion loss and in circuit size and has a good performance for IC integration in respect of a step attenuator capable of stepwise changing the quantity of attenuation to a required value. Plural FET switches for passing/interrupting an input signal are connected between an input terminal and an output terminal and fixed attenuators with optional attenuation values are arranged in parallel with switches. Such circuits are connected in cascade, respective FET switches are selectively turned on/off so as to obtain a required attenuation value. Since the total number of switches and the number of signal passing switches can be reduced as compared with a conventional attenuator, this step attenuator can be realized on a smaller chip area and has a smaller insertion loss.

The JP-A-07-087024 discloses an optical receiver to extend the dynamic range of the optical receiver by suppressing deterioration in the optical receiver such as distortion of the output of the receiver when the power of a received light is high. A step attenuator is inserted to a pre-stage of a first stage amplifier and a variable attenuator is inserted to a post-stage. The input level of the first stage amplifier is attenuated by decreasing the attenuation of the step attenuator when the power of the received light is small and by increasing the attenuation of the step attenuator when the power of the received light is high thereby suppressing the distortion produced as a stage amplifier.

The JP-A-10-173464, the JP-A-07-249954 and the JP-A-07-087024 are also designed for fixed input and output impedances.

In a conventional CATV system (Common Antenna Television System), the system gets the information signals from an antenna unit connected to the head end which converts the electrical signals into optical signals and sends the optical signals by a transmitter through a glass-fiber cable to the primary hub. The primary hub receives the optical signal from the head end and transmits it to a secondary hub which converts the optical signal into a RF-signal. The RF-signal is transmitted over a coaxial cable to the consumers. The problem with such a system is that commonly used gain control circuits,

used in optical receivers, distorts the information signals. Therefore several investigations have been done to reduce such distortion occurring in the optical receiver.

It is an objective of the invention to provide an optical receiver circuit which is improved with respect to intermodulation distortion and provides a constant output signal level.

For achieving this objective, an optical receiver circuit of the invention comprises an optical converter circuit converting optical power to electrical power; a sensor circuit detecting a characteristic value of the electric power; and an attenuator circuit having a variable attenuation, the attenuation being controlled by the characteristic value of the electric power output by the sensor circuit to obtain a constant output signal level of the optical receiver circuit and an output circuit. A distortion free, automatic gain control circuit can be made by sensing the optical input signal level and switching the attenuator circuit with the output of the sensor circuit. This optical receiver circuit has a substantially reduced intermodulation distortion and is, therefore, particularly adapted for a CATV optical receiver.

According to a preferred embodiment of the invention, the optical converter circuit comprises a photo diode. Which has proven to be the best possible way of converting optical power to electrical power.

According to a further preferred embodiment of the invention, the sensor circuit comprises a resistor network connected to the optical converter circuit for deriving a control voltage V_{CONTR} as a characteristic value of the electric power output by the optical converter circuit. Such a resistor network connected to the optical converter circuit, is a reliable and simple way of deriving the control voltage V_{CONTR} as a characteristic value of the electric power output.

According to a further preferred embodiment of the invention, the attenuator circuit is a step attenuator circuit comprising a plurality of attenuator stages which are selectively switchable into active states. By selectively switching individual attenuator stages either one by one or in groups into active states, a wide variety of attenuation values can advantageously be obtained with a minimum number of attenuator stages.

According to a further preferred embodiment of the invention, the sensor circuit comprises an A/D converter converting the control voltage V_{CONTR} to a digital signal controlling the attenuator stages of the attenuator circuit. A distortion free, automatic gain control circuit can advantageously be made by sensing the optical input signal level with the

input of an A/D converter and switching the attenuator circuits with the output of the A/D-converter.

According to a further preferred embodiment of the invention, the attenuator stages have different attenuation values each. By selectively switching individual attenuator stages having different attenuation values either one by one or in groups into active states, the range of the attenuation values can advantageously be further expanded with a minimum number of attenuator stages.

According to a further preferred embodiment of the invention, the attenuator stages are T-type attenuator stages comprising a resistor and a semiconductor switch in series with the resistor. With a T-type attenuator stage the insertion loss can advantageously be lowered.

According to a further preferred embodiment of the invention, the attenuator stages are T-type attenuator stages comprising two resistors and a semiconductor switch in series with the resistors, and wherein one of the resistors is bridged by another semiconductor switch. This advantageously allows variation of the attenuation of one and the same attenuation stage.

According to a further preferred embodiment of the invention, capacitors are provided for separating respective input end, of the attenuator stages and an input capacitor for coupling the input end of said attenuator stages to an output of the optical receiver circuit and an output capacitor for coupling an output of the attenuator circuit to the output circuit.

According to a further preferred embodiment of the invention, the semiconductor switches are MOSFET's which are advantageously controllable by the outputs of for example a A/D converter and which also have advantages in respect to integration on a chip.

According to a further preferred embodiment of the invention, the output circuit comprises a matching network, an amplifier stage and an output transformer which advantageously complete the optical receiver circuit.

These and various other advantages and features of novelty which characterize the present invention are pointed out with particularity in the claims annexed hereto and forming a part hereof. However, for a better understanding of the invention, its advantages, and the object obtained by its use, reference should be made to the drawings which form a further part hereof, and to the accompanying descriptive matter in which there are illustrated and described preferred embodiments of the present invention.

In the drawings:

Fig. 1 shows a present CATV system;

Fig. 2 shows a block diagram of an optical receiver unit;

Fig. 3 shows a circuit diagram of the attenuator circuit according to the present invention; and

Fig. 4 shows a graph of the second order distortion (d2) as function of the optical input power.

Fig. 1 shows a diagram of a present CATV system. The system gets the information signals from an antenna unit 2 and/or a network backbone 4. The antenna unit 2 and/or the network backbone 4 are connected to the head end 12. The head end 12 converts all signals into an optical signal and sends the optical signals over a glass-fiber cable, a so-called fiber backbone 14, to a primary hubs 6, 8 and 10. The primary hubs 6, 8 or 10 receive the optical signal from the head end 12 and transmit the optical signal over a secondary ring 18, a so-called fiber ring, to secondary hubs 16, 20.

The secondary hubs or optical receiver circuits 16,20 receive the optical signal of the primary hubs and convert the optical signal into an RF-signal. The RF-signal is transmitted over a coaxial cable 25 and RF-amplifiers 22, 24 over a so-called last mile 26 to the consumers, i.e. houses 28, 30, 32. In the houses there are residential gateways and in-house communication networks. This is in principle shown in the house 28. There is shown a residential gateway 34. For instance a computer, telephone and a game gear are coupled with the residential gateway 34 for in-house communication and communication with the outside world.

Fig. 2 shows a block diagram of an optical receiver circuits. The optical receiver circuit, for example the optical receiver circuit 20, receives the optical signal via an input terminal 36. The input terminal 36 is connected to an optical converter circuit 38. The optical converter circuit 38 is connected to a bias voltage by a terminal 40 and to the ground voltage by a terminal 42. The optical converter circuit 38 converts the optical signal to an electrical signal. The optical converter circuit 38 comprises a photo diode to convert the optical signal to an electrical signal.

The electrical signal of the optical converter circuit 38 is transmitted to an attenuator circuit 44. The attenuator circuit 44 attenuates the electrical signal of the optical

converter circuit 38 in order to provide constant signal levels at its output to a matching network 46. The matching network 46 matches the output of the attenuator circuit 44 to an amplifier stage 48. The amplifier stage 48 comprises two amplifiers 54, 56 in order to amplify the output signal of the matching network for an output transformer 50. The output transformer 50 transforms the balanced signal of its input to an unbalanced signal at its output 52. The matching network 46, the amplifier stage 48 and the output transformer 50 form the output circuit.

Fig. 3 shows a circuit diagram of the attenuator circuit 44. A light controlled current source 56, which is represented by a photo diode, is connected in parallel to two input terminals of the attenuator circuit 44. A load impedance 108 (270 Ω) is connected at the output terminals of the attenuator circuit. In order to operate the light controlled current source 56, a resistor 54 is connected between a bias voltage supply and the light controlled current source 56. On the other side of the light controlled current source 56 a resistor 58 is connected between the light controlled current source 56 and ground. At the resistor 58, a voltage is measured which is supplied by a resistor 60 and a comparator/level setting circuit 62 to an analogue to digital A/D converter 64.

The comparator/level setting circuit 62 creates a control voltage V_{CONTR} for the A/D-converter 64. V_{CONTR} determines the output signal of the A/D-converter 64 for the attenuation stages of the attenuation circuit 44. An output 66 of the A/D-converter 64 is coupled to a terminal 68 of a first attenuation stage. The first attenuation stage comprise a serial circuit of a resistor 86 with the resistance value of 3000 Ω and a MOSFET 88. The terminal 68 is connected between the resistor 86 and the drain of the MOSFET 88. The gate contact of the MOSFET 88 is connected to ground. The attenuation stage is connected in parallel to the light controlled current source 56.

The light controlled current source 56 and the first attenuation stage are separated by two capacitances 110 and 130. A terminal 70 of the A/D-converter 64 is coupled to a terminal 72 of a second attenuation stage. The second attenuation stage comprise a serial circuit comprising a resistor 90 with the resistance value of 1400 Ω and a MOSFET 92. The terminal 72 is connected between the resistor 90 and the drain contact of the MOSFET 92. The first and second attenuation stages are separated by capacitances 112 and 132.

The second attenuation stage is in parallel to the light controlled current source 56. The gate contact of the MOSFET 92 is connected to ground. A terminal 74 of the A/D-converter 64 is coupled to a terminal 76 of the third attenuation stage. The third attenuation

stage is in parallel to the light controlled current source 56. The second and the third attenuation stages are separated by capacitances 122 and 134.

The third attenuation stage comprise a serial circuit comprising a resistor 94 with the resistance value of 500 Ω, a resistor 96 with the resistance value of 220 Ω and a MOSFET 98. A terminal 76 is connected between the resistor 96 and the drain contact of the MOSFET 98. The gate contact of the MOSFET 98 is connected to ground. A further MOSFET 100 is connected in parallel to the resistor 96. The resistor 96 and the MOSFET 100 are separated by capacitances 142 and 144. The capacitance 142 is connected between the resistor 96 and the drain contact of the MOSFET 98. The capacitance 144 is connected between the resistor 94 and the resistor 96. The gate contact of the MOSFET 100 is connected to ground. The terminal 78 of the A/D-converter 64 is coupled to the terminal 80 of the fourth attenuation stage.

The fourth attenuation stage is in parallel to the light controlled current source 56. The fourth attenuation stage comprise a serial circuit comprising a resistor 102 with the resistance value of 325 Ω and a MOSFET 104. The terminal 80 is connected between the resistor 102 and the drain contact of the MOSFET 104. The gate of the MOSFET 104 is connected to ground. The terminal 80 is connected between the resistor 102 and the drain contact of the MOSFET 104. The third and fourth attenuation stages are separated by the capacitances 124 and 136. The drain contact of the MOSFET 100 is connected to the terminal 80. A terminal 82 of the A/D-converter 64 is coupled to a terminal 84 of the fifth attenuation stage.

The fifth attenuation stage comprise a serial circuit comprising a resistor 106 with a resistance value of 130 Ω and a MOSFET 109. The fourth and fifth attenuation stages are separated by capacitances 126 and 138. The fifth attenuation stage is in parallel to the light controlled current source 56. The gate contact of the MOSFET 109 is connected to ground. A terminal 84 is connected between a resistor 106 and the drain contact of the MOSFET 109. The fifth attenuation stage and a load 108 are separated by capacitances 128 and 140. Depending on the value of V_{CONTR} the attenuation stages are set by the A/D-converter 64 and the attenuation is therefore determined by the division of the current of the current source section 56 between the attenuation stages and the load 108. Furthermore an advantageous feature of the attenuator circuit is that the attenuator circuit reduces the intermodulation distortion of the optical receiver.

The MOSFETS 88, 92, 98, 100, 104 and 109 are of the same type. This type of MOSFET has a high-ohmic resistance at a gate source voltage of 5 V and has a low-ohmic

resistance (around 10 Ω) at a gate source voltage of 0 V. At a gate source voltage, ranging from 2 V up to 2,8 V, the FET resistance is moving linear from a low ohmic resistance to a high ohmic resistance. After connecting the MOSFET in series of a resistor of for example 250 Ω, between the push and pull side, the responsivity of the optical receiver unit can be adjusted by an external voltage.

The attenuator circuit built with the above described MOSFET shows that this field effect transistor can be used as a switch. With a switch, a resistor can be connected or disconnected in the optical receiver circuit. By placing several switches with different resistor values in this module, a step attenuator can be built. With a step size of 0.5 dB of electrical attenuation, the attenuator is adjusted each 0.25 dB step of optical input power. This means that with an increasing optical input power the electrical output is a saw signal with an amplitude of 0.5 dB (theoretically).

The function of the MOSFET 100 is more complex than the function of the other MOSFETs. The MOSFET 100 creates an attenuation of 6 dB by the resistor 102 (325 Ω), giving 4 dB attenuation, in parallel with the resistor 94 (500 Ω), giving an additional attenuation of 2 dB. The serial circuit of the resistor 94 (500 Ω) and the resistor 96 (220 Ω) creates an attenuation of 2 dB when the resistor 102 (325 Ω) is not connected. To have the difference between 500 Ω and 720 Ω, an extra MOSFET 100 is used to short circuit the resistor 96 (220 Ω) in the case that MOSFET 104 is activated (= attenuation > 4 dB).

A distortion free automatic gain control circuit can be made by sensing the optical input power with the input of an A/D-converter 64 and switching the MOSFETS 88, 92, 98, 100, 104, 109 with the output of the A/D-converter 64.This circuit has a step size of 0.5 dB and a range of 9 dB (both electrical).

This circuit is placed between the optical converter circuit 38 and the output circuit comprising the matching network 46, the amplifier stage 48 and the output transformer 50. The signals in the attenuator circuit are balanced. The attenuator circuit is placed between the push and pull side.

Fig. 4 shows a graph of the second order distortion (d2) in dBc as function of the optical input power in dBm. The second order distortion (d2) is defined by the second order distortion product which is the difference in dB between the peak level of an RF signal at the measurement frequency, and the peak level of the signal at the measuring frequency caused by two CW signals with their second order modulation product (f1 ± f2) at the measuring frequency.

The graph "d2 without attenuation" rises linear with rising optical input power. The graph "d2 with attenuation" shows a shape which rises to a maximum value and moves vertically down after reaching the maximum in the case of further increasing of optical input power. The graph slopes linearly up until it reaches again a maximum value. After reaching the maximum value the graph moves again vertically down to another lower value in the case of further increasing of an optical input power and then the graph slopes up again. The average value of the before described attenuation forms a horizontal line in the case of optical input power. This horizontal line is shown by the line indicated with "average of d2 with attenuation".

The maximum variation of the response above 0 dBm optical input power is 0.8 dBmV. The maximum variation above 0 dBm optical input power is 1.6 dB. The response and the shown shape of attenuation "d2 with attenuation" (both at low frequences) are "as good as" constant above the threshold point. The actual attenuation value is equal to the attenuation of a standard part without gain control. With the described optical receiver circuit with optical gain control which consists out of a step attenuator, the optical receiver circuit can be made with an optical adjustment range of for example 2 dB. The use of MOSFETS with a lower capacitance can improve the variation at the response curve as function of optical input signal level.

New characteristics and advantages of the invention covered by this document have been set fourth in the foregoing description. It will be understood, however, that this disclosure is, in many respects, only illustrative. Changes may be made in details, particularly in matters of shape, size, and arrangement of parts, without exceeding the scope of the invention. The scope of the invention is, of course, defined in the language in which the appended claims are expressed.

CLAIMS:

1. Optical receiver circuit comprising:
an optical converter circuit converting optical power to electrical power;
a sensor circuit detecting a characteristic value of the electric power;
an attenuator circuit having a variable attenuation, the attenuation being controlled by the characteristic value of the electric power output by the sensor circuit to obtain a constant output signal level of the optical receiver circuit; and
an output circuit.

2. Optical receiver circuit of claim 1 wherein the optical converter circuit comprises a photo diode.

3. Optical receiver circuit according to claim 1, wherein the sensor circuit comprises a resistor network connected to the optical converter circuit for deriving a control voltage V_{CONTR} as the characteristic value of the electric power output by the optical converter circuit.

4. Optical receiver circuit of claim 1, wherein the attenuator circuit is a step attenuator circuit comprising a plurality of attenuator stages which are selectively switchable into active states.

5. Optical receiver circuit according to claim 4, wherein the sensor circuit comprises an A/D converter converting the control voltage V_{CONTR} to a digital signal controlling the attenuator stages of the attenuator circuit.

6. Optical receiver circuit of claim 4, wherein the attenuator stages have different attenuation values each.

7. Optical receiver circuit of any of the claims 1 and 4 to 6, wherein the attenuator stages are T-type attenuator stages comprising a resistor and a semiconductor switch in series with the resistor.

8. Optical receiver circuit of any of the claims 1 and 4 to 6, wherein the attenuator stages are T-type attenuator stages comprising two resistors and a semiconductor switch in series with the resistors and wherein one of the resistors is bridged by another semiconductor switch.

9. Optical receiver circuit of claim 7 or 8, wherein capacitors are provided for separating respective input end, of the attenuator stages and an input capacitor for coupling the input end of said attenuator stages to an output of the optical receiver circuit and an output capacitor for coupling an output of the attenuator circuit to the output circuit.

10. Optical receiver circuit of any of the claims 7 to 9, wherein the semiconductor switches are MOSFETs.

11. Optical receiver circuit of claim 1, wherein the output circuit comprises a matching network, an amplifier stage and an output transformer.

ABSTRACT:

Optical receiver circuit comprising an optical converter circuit (38) comprising a photo diode and converting optical power to electrical power; a sensor circuit for deriving a control voltage V_{CONTR} as a characteristic value of the electric power output by the optical converter circuit (38); an attenuator circuit (44) having a variable attenuation, the attenuation being controlled by the characteristic value of the electric power output by the sensor circuit to obtain a constant output signal level of the optical receiver circuit. An output circuit comprises a matching network (46), an amplifier stage (48) and an output transformer (50).

Fig. 3

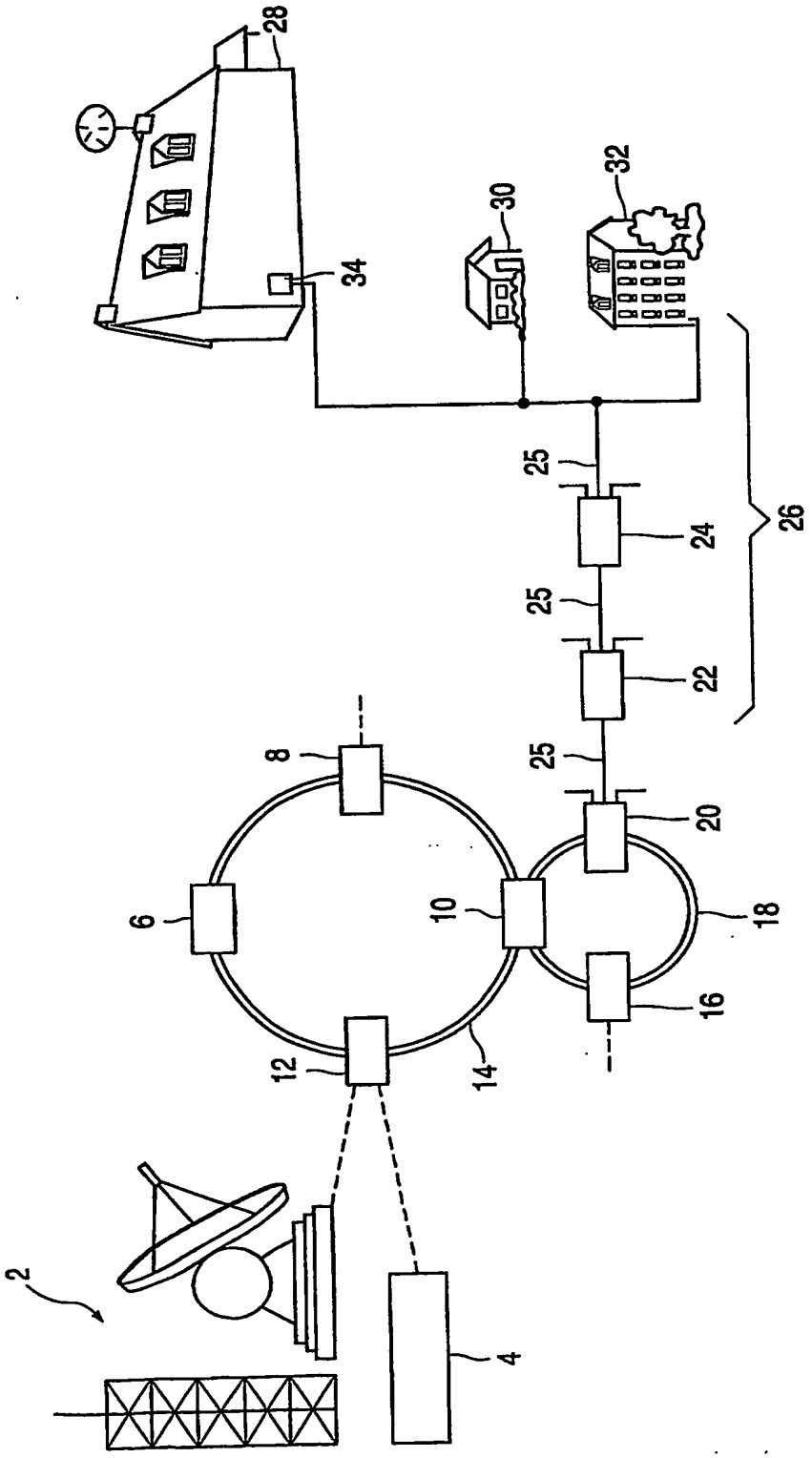

FIG. 1

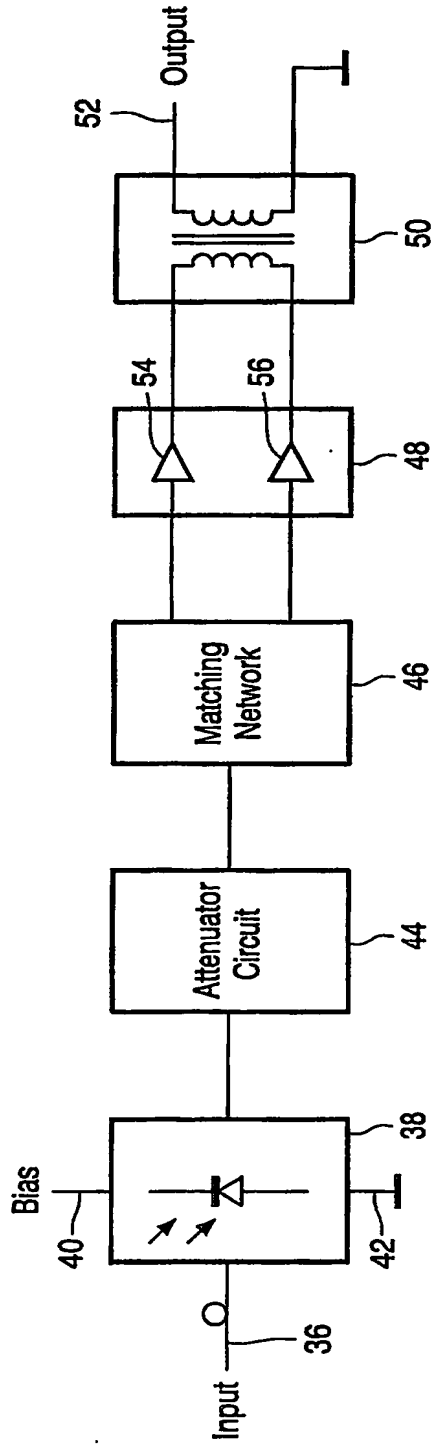
Output
52
50
54
56
48
Matching Network
46
Attenuator Circuit
44
38
Bias
40
42
36
Input

FIG. 2

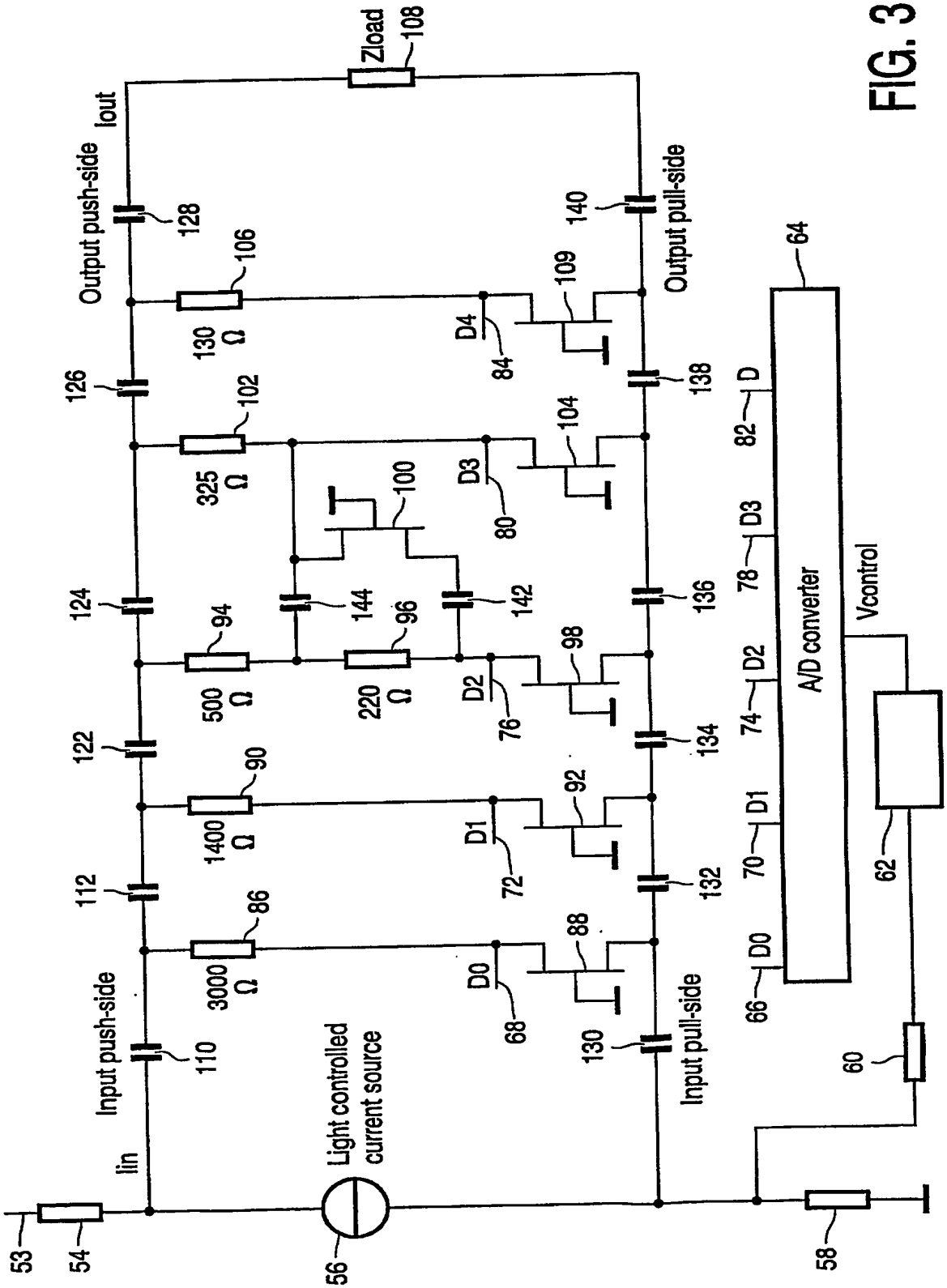
Zload
108
Iout
Output push-side
Output pull-side
128
140
106
109
130 Ω
D4
84
126
138
102
104
325 Ω
D3
80
100
124
136
94
144
96
142
500 Ω
220 Ω
D2
76
98
122
134
90
92
1400 Ω
D1
72
112
132
86
88
3000 Ω
D0
68
Input push-side
Input pull-side
110
130
Iin
Light controlled
current source
53
54
56
58
60
62
64
A/D converter
Vcontrol
D
82
D3
78
D2
74
D1
70
D0
66

FIG. 3

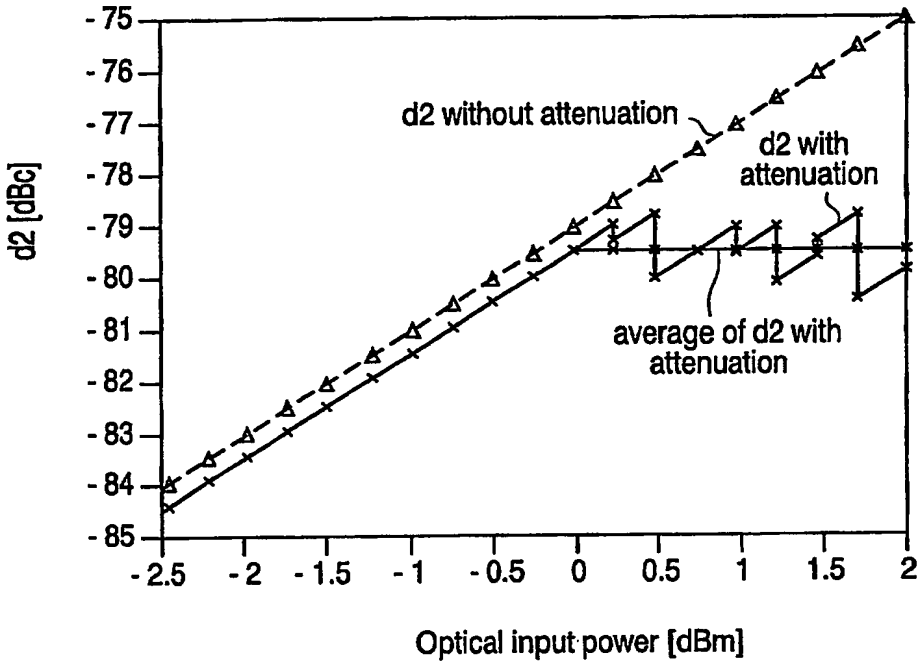
- 75
- 76
- 77
- 78
- 79
- 80
- 81
- 82
- 83
- 84
- 85
d2 [dBc]
d2 without attenuation
d2 with attenuation
average of d2 with attenuation
- 2.5
- 2
- 1.5
- 1
- 0.5
0
0.5
1
1.5
2
Optical input power [dBm]

FIG. 4